**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers formed around the external terminals, the insulating layers formed on the interconnect pattern, the insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer.

2. (Original) The semiconductor device as defined in claim 1,

wherein at least one of the plurality of insulating layers has a stress relieving function.

3. (Original) The semiconductor device as defined in claim 1,

wherein at least one of the plurality of insulating layers is formed of a resin.

4. (Previously Presented) The semiconductor device as defined in claim 1,

wherein the insulating layers contact the external terminals at opening portions each of which has an inclined surface providing a taper increasing in size from the second layer to the first layer.

5. (Original) The semiconductor device as defined in claim 1,

wherein each of the external terminals includes a base and a connection portion provided on the base; and

wherein the base is provided in an opening portion through which each of the external terminals contact the insulating layers.

6. (Original) The semiconductor device as defined in claim 1,

wherein the insulating layers contact the external terminals at opening portions each of which is formed with a curved surface.

7. (Original) The semiconductor device as defined in claim 1,

wherein the interconnect pattern is formed on a stress relieving layer formed below the plurality of insulating layers.

8. (Previously Presented) The semiconductor device as defined in claim 1,

wherein the uppermost layer of the insulating layers is formed over the whole surface of a layer just under the uppermost layer, the uppermost layer formed in a region except for an area of the external terminals.

9. (Previously Presented) The semiconductor device as defined in claim 1,

wherein the uppermost layer of the insulating layers has its area smaller than an area of a layer just under the uppermost layer.

10-12. (Canceled)

13. (Currently Amended) ~~The semiconductor device as defined in claim 1~~A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer,

wherein the interconnect pattern is formed on the uppermost layer of the insulating layers, the uppermost layer having protrusions and depressions; and

wherein the external terminals are formed in the depressions and the external terminals are electrically connected to the interconnect pattern in the depressions.

14. (Previously Presented) The semiconductor device as defined in claim 13, wherein the insulating layers have a stress relieving function.

15. (Previously Presented) The semiconductor device as defined in claim 13, wherein the insulating layers are formed of a resin.

16. (Original) The semiconductor device as defined in claim 13,

wherein each of the external terminals includes a base and a connection portion provided on the base; and

wherein the base and the interconnect pattern are constructed as a single member.

17. (Original) The semiconductor device as defined in claim 13,

wherein each of the depressions is formed to have an opening extremity larger than the bottom.

18-19. (Canceled)

20. (Previously Presented) The semiconductor device as defined in claim 13, wherein a protective film is formed on the uppermost layer.

21. (Currently Amended) A circuit board on which is mounted a semiconductor device, the semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers formed around the external terminals, the insulating layers formed on the interconnect pattern, the insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer.

22. (Currently Amended) ~~The circuit board as defined in claim 21~~A circuit board on which is mounted a semiconductor device, the semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer,

wherein the interconnect pattern is formed on the uppermost layer of the insulating layers, the uppermost layer having protrusions and depressions; and

wherein the external terminals are formed in the depressions and the external terminals are electrically connected to the interconnect pattern in the depressions.

23. (Currently Amended) An electronic instrument having a semiconductor device, the semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers formed around the external terminals, the insulating layers formed on the interconnect pattern, the insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer.

24. (Currently Amended) ~~The electronic instrument as defined in claim 23~~An electronic instrument having a semiconductor device, the semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the coefficient of thermal expansion of the first layer is greater than the coefficient of thermal expansion of the second layer,

wherein the interconnect pattern is formed on the uppermost layer of the insulating layers, the uppermost layer having protrusions and depressions; and

wherein the external terminals are formed in the depressions and the external terminals are electrically connected to the interconnect pattern in the depressions.

25. (Withdrawn) A method of manufacture of a semiconductor device comprising the steps of:

forming an interconnect pattern electrically connected to a plurality of electrodes of a semiconductor element;

forming external terminals on the interconnect pattern; and

forming a plurality of insulating layers around the external terminals, over the interconnect pattern.

26. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 25,

wherein in the step of forming the insulating layers, opening portions which are used for contacting the external terminals and constituted by first and second holes, are formed in the insulating layers which include first and second insulating layers;

wherein the first insulating layer is formed; the first holes are formed in the first insulating layer; the second insulating layer is formed over the first holes and the first insulating layer; and the second holes are formed in the second insulating layer over the first holes; and

wherein the external terminals are formed after forming the insulating layers.

27. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 25,

wherein at least one of the plurality of insulating layers is formed to have a stress relieving function.

28. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 25,

wherein at least one of the plurality of insulating layers is formed of a resin.

29. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 25,

wherein the insulating layers are formed to include an upper layer and a lower layer of different characteristics.

30. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 29,

wherein the Young's modulus of the lower layer of the insulating layers is made larger than the Young's modulus of the upper layer of the insulating layers.

31. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 29,

wherein the coefficient of thermal expansion of the upper layer of the insulating layers is made larger than the coefficient of thermal expansion of the lower layer of the insulating layers.

32. (Withdrawn) A method of manufacture of a semiconductor device, comprising the steps of:

forming an insulating layer on a semiconductor element, the insulating layer comprising at least one layer and having protrusions and depressions;

forming an interconnect pattern on the insulating layer, the interconnect pattern being connected to a plurality of electrodes of the semiconductor element; and

forming external terminals in the depressions, the external terminals being electrically connected to the interconnect pattern.

33. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 32,

wherein a base which is a bottom portion of each of the external terminals is formed on an inner surface of each of the depressions, as a single member with the interconnect pattern; and

wherein each of the external terminals is formed by providing a connection portion on the base.

34. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 32,

wherein the insulating layer is formed to have a stress relieving function.

35. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 32,

wherein the insulating layer is formed of a resin.

36. (Withdrawn) The method of manufacture of a semiconductor device as defined in claim 32,

wherein a protective film is formed on the uppermost layer of the semiconductor device.

37-38. (Canceled)

39. (Currently Amended) A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers formed around the external terminals, the insulating layers formed on the interconnect pattern, the insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the Young's modulus of the second layer is greater than the Young's modulus of the first layer.

40. (Previously Presented) The semiconductor device as defined in claim 39, wherein at least one of the plurality of insulating layers has a stress relieving function.

41. (Previously Presented) The semiconductor device as defined in claim 39, wherein at least one of the plurality of insulating layers is formed of a resin.

42. (Previously Presented) The semiconductor device as defined in claim 39, wherein the insulating layers contact the external terminals at opening portions each of which has an inclined surface providing a taper increasing in size from the second layer to the first layer.

43. (Previously Presented) The semiconductor device as defined in claim 39, wherein each of the external terminals includes a base and a connection portion provided on the base; and

wherein the base is provided in an opening portion through which each of the external terminals contact the insulating layers.

44. (Previously Presented) The semiconductor device as defined in claim 39, wherein the insulating layers contact the external terminals at opening portions each of which is formed with a curved surface.

45. (Previously Presented) The semiconductor device as defined in claim 39, wherein the interconnect pattern is formed on a stress relieving layer formed below the plurality of insulating layers.

46. (Previously Presented) The semiconductor device as defined in claim 39, wherein the uppermost layer of the insulating layers is formed over the whole surface of a layer just under the uppermost layer, the uppermost layer formed in a region except for an area of the external terminals.

47. (Previously Presented) The semiconductor device as defined in claim 39,

wherein the uppermost layer of the insulating layers has its area smaller than an area of a layer just under the uppermost layer.

48. (Currently Amended) A circuit board on which is mounted a semiconductor device, the semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers formed around the external terminals, the insulating layers formed on the interconnect pattern, the insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the Young's modulus of the second layer is greater than the Young's modulus of the first layer.

49. (Currently Amended) An electronic instrument having a semiconductor device, the semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes;

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes; and

a plurality of insulating layers formed around the external terminals, the insulating layers formed on the interconnect pattern, the insulating layers including a first layer, the insulating layers including a second layer formed closer to the semiconductor element than the first layer,

wherein the Young's modulus of the second layer is greater than the Young's modulus of the first layer.